REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of October 31, 2006 is respectfully requested.

Claims 14-35 were pending and treated in the outstanding Office Action. In this regard, the Examiner again indicated that claims 14 and 18-23 were allowed. As those claims have not been modified by this amendment, it is submitted that those claims are therefore still in condition for allowance. However, the Examiner withdrew the previous indication that claims 15, 16, and 24-35 were also allowed, and rejected those claims as being either anticipated by or unpatentable over the Enomoto reference (U.S. Publication 2003/0032284). However, the rejected claims have now been amended as indicated above. For the reasons discussed below, it is submitted that these claims are now in condition for allowance.

As explained on page 2, lines 10-27 of the original specification, stresses are generated between layers of a gate electrode, which could cause the layers to peel apart. Specifically, the sides of the gate electrode are abnormally oxidized, causing the peeling. The present invention has been developed to address this problem.

As now recited in independent claims 15, 16, 24, and 31, a gate electrode having a metallic silicide layer, a metallic polysilicon layer under the metallic silicide layer, and an SiN layer on the metallic silicide layer is formed on a semiconductor substrate (see Figure 1(b) and page 6, lines 2-15 of the original specification). Then, a spacer consisting of an oxide film is formed on *a side wall of the metallic polysilicon layer and the metallic silicide layer* of the gate electrode (see Figure 1(d) and page 7, lines 15-22 of the original specification). As a result, the side walls of the metallic polysilicon layer and the metallic silicide layer are protected from abnormal oxidation and peeling.

The Enomoto reference teaches a method of fabricating a semiconductor integrated circuit device. However, the Enomoto reference does not teach or even suggest forming a gate electrode on a semiconductor substrate, in which the gate electrode has a metallic silicide layer, a metallic polysilicon layer under the metallic silicide layer, and an SiN layer on the metallic silicide layer, and in which a spacer consisting of an oxide film is formed on a side wall of the

metallic polysilicon layer and the metallic silicide layer of the gate electrode. Because there is not even a suggestion of this feature, one of ordinary skill in the art would not be motivated to modify the Enomoto reference to obtain the invention recited in amended independent claims 15, 16, 24, and 31. Accordingly, it is respectfully submitted that amended independent claim 15, 16, 24, and 31, and the claims that depend therefrom, are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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February 28, 2007